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EXAMINER
YAM, STEPHEN K

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/783,007	FUJINO, JUNJI	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This action is in response to Amendments and remarks filed on July 18, 2002. Claims 1, 2, 4-9, and 11-15 are currently pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In Claim 15, "the first and second conductivity patterns" lack proper antecedent basis.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, and 9 are rejected under 35 U.S.C. 102(b) as being unpatentable by Sawada et al. US Patent No. 5,652,425.

Regarding Claims 1 and 9, Sawada et al. teach a photoelectric conversion and amplification device comprising a photoelectric conversion circuit (Fig. 1) (see Col. 1, lines 6-8 and abstract), an amplifier (600) (see Fig. 3) with a first input terminal (V_{in1}) and a second input

terminal (V_{in2}) and amplifying and outputting a difference between electric signals fed to the first and second input terminals, a first wire (36) (see Fig. 4) connecting the photoelectric conversion circuit to the first input terminal (see Fig. 1 and 4) and a second wire (37) connecting the second output on the photoelectric conversion circuit to the second input terminal (see Fig. 1 and 4), where the first and second wires have substantially identical lengths and are substantially parallel (see Fig. 5). Since electrodes are generally used to attach two separate circuits, it is inherent that electrodes are connected to the outputs of the two preamplifiers, at Fig. 1, ref. 4b & 6b to interconnect the two components of Sawada's invention, and both wires are connected both electrically and physically to the photoelectric conversion circuit. Regarding claim 9, "an infrared communication device" cannot be given any patentable weight since the body of the claim does not claim such structure (see also, Sawada et al: Col. 1, lines 10-11).

Regarding Claim 2, Sawada also teaches (see Fig. 1) identical bias voltages (V_{PD}) applied to the first and second input terminals.

Regarding Claim 4, since the two wires (36, 37) are substantially parallel and substantially of identical length, the distance between the first electrode and the first input terminal is substantially identical to the distance between the second electrode and the second input terminal, and the distance between the first and second electrode is substantially identical to the distance between the first and second input terminals.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. over Agarwal US Patent No. 6,175,438.

Sawada et al. teach the invention as taught in the previous paragraph for Claim 1. Sawada et al. also teach (see Fig. 1) the first electrode connected electrically to one end of the photodiode. Applicant defines "electrically open" as "not directly connected to the current signal obtained as a result of photoelectric conversion performed in the photodiode chip" (see Page 8, lines 18-20 of the Applicant's specification)- therefore, Sawada et al. teach (see Fig. 1) the second electrode electrically open, as the second electrode is connected to the capacitor and is not associated with the photoelectric conversion performed in the photodiode. Sawada et al. do not teach the specific photodiode type. Agarwal teaches the use of a CMOS semiconductor, consisting of a N-type semiconductor and P-type semiconductor, in Column 1, line 46-50, for a photodiode chip for photoelectric purposes. It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the invention of Sawada et al. with CMOS technology taught by Agarwal, as CMOS is widely used and recognized as an effective photodiode.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. over Liang et al. US Patent No. 5,781,233.

Sawada et al. teach the invention as taught in the previous paragraph for Claim 1. Sawada et al. also teach (see Fig. 1) the first electrode connected electrically to one end of the

photodiode. The Applicant defines "electrically open" as "not directly connected to the current signal obtained as a result of photoelectric conversion performed in the photodiode chip" (see Page 8, lines 18-20 of the Applicant's specification)- therefore, Sawada et al. teach (see Fig. 1) the second electrode electrically open, as the second electrode is connected to the capacitor and is not associated with the photoelectric conversion performed in the photodiode. Sawada et al. do not teach the specific photodiode type, and do not teach the dummy photodiode as a diode with an N-type semiconductor and a P-type semiconductor joined together. Liang et al. teach (see Fig. 2B) a photodiode with a first region (D,GX) formed by joining a P-type semiconductor substrate (35) with an N-type semiconductor (D_b). Liang et al. also teach (see Fig. 11B) a dummy photodiode with a second region (D,GX) formed by joining a P-type semiconductor substrate (35) with an N-type semiconductor (D_b), where the dummy photodiode shielded from light by a metal plate (MN) covering the top portion of the dummy photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dummy photodiode of Liang et al. with the invention of Sawada et al., to match the wire impedance with an exact photodiode match for improved interference capture.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. in view of Watannabe US Patent No. 5,132,532.

Sawada et al. teach the invention as taught in the previous paragraph for Claim 1. Sawada et al. does not teach a substrate having a first conductor pattern and a second conductor pattern where the photoelectric conversion circuit and the amplifier circuit are mounted, wherein the first wire connects the first electrode to the first input terminal by way of the first conductor pattern and

the second wire connects the second electrode to the second input terminal by way of the second electrode pattern. Sawada et al. also does not teach a first-bonding operation performed on the first and second elements and a second-bonding operation performed on the first and second conductor patterns, respectively. Watanabe teaches (see Fig. 3) a photoelectric converter module comprising a substrate (43) to mount a photoelectric conversion circuit (11, 30) and an amplified circuit (20) with a first (31a) (see Fig. 4A) and second (31b) conductor pattern, and bonding wires (22) (see Col. 4, lines 42-47) to connect the conductor patterns to the amplifier (20). Regarding Claim 7, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Sawada et al. in view of Nishiyama with the connection methods taught by Watanabe, to provide an integral photodiode/amplification device. Regarding Claim 8, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the two wires as two separate bonding operations in the invention of Sawada et al. in view of Nishiyama, as two separate electrical connections are being bonded, providing a lowered risk of chip damage.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. in view of Nishiyama US Patent No. 5,610,395.

Sawada et al. teach a photoelectric conversion and amplification device that converts an optical signal into an electric signal (see Col. 1, lines 6-8 and abstract) with attachment of the photoelectric conversion circuit (see Fig. 1) to the amplifier, as described in the outputs (7, 8) (see Fig. 1) to the inputs of the amplifier (see extension of (7,8) on Fig. 1 and 3). Since electrodes are generally used to attach two separate circuits, it is well known that electrodes are

connected to the outputs of the two preamplifiers, at Fig. 1, ref. 4b & 6b to interconnect the two components of Sawada's invention. Sawada furthermore teaches (see Col. 6, lines 12-16) a first wire connecting the photoelectric output (7, 36) (see Fig. 1 and 4) to the first input of the amplification circuit (see Fig. 3) and a second wire connecting the dummy output (8, 37) (see Fig. 1 and 4) to the second input of the amplification circuit (see Fig. 3), where the first and second wire have substantially identical lengths and are substantially parallel. Sawada also teaches the use of identical bias voltages through a bias circuit (2) (see Fig. 1 and Col. 2, line 52) to supply a voltage of V_{PD} to both a light-receiving element and a capacitor with an equivalent capacitance to the light-receiving element, so bias voltages at both inputs of the differential amplifier are identical. Sawada does not teach a first chip containing the photoelectric conversion circuit and a second chip containing the amplifier circuit. Nishiyama teaches (see Fig. 1) a photodetector module with a first chip (2,3) containing a photoelectric conversion circuit and a second chip (4) having an amplifier circuit. Since the first chip contains a photodiode, it is well known to include electrodes to electrically connect the chip to other processing elements which receive the outputs of the chip. Since the second chip is an IC (see Col. 2, lines 38-40), the chip requires input terminals to receive an electrical signal from the photoelectric conversion circuit, and since two inputs are received from the photoelectric conversion circuit, two input terminals are located on the second chip to connect to the photoelectric conversion circuit. Nishiyama also teaches the second input terminal in close proximity to the first input terminal, and it is well known that the input terminals are eventually connected to the two inputs on the amplifier device within the second chip. Nishiyama also teaches (see Fig. 1) the distance between the first electrode and the first input terminal to be

substantially identical to the distance between the second electrode and the second input terminal, and the distance between the first and second electrodes to be substantially identical to the distance between the first and second input terminals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the physical configuration of Nishiyama in the device of Sawada et al., to minimize physical space in mounting the two chips to a common base.

10. Claims 12 and 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. in view of Nishiyama as applied to claim 11 above, and further in view of Liang et al.

Regarding Claim 12, Sawada et al. in view of Nishiyama teach the invention as taught in the previous paragraph for Claim 11. Applicant defines "electrically open" as "not directly connected to the current signal obtained as a result of photoelectric conversion performed in the photodiode chip" (see Page 8, lines 18-20 of the Applicant's specification)- therefore, Sawada et al. teach (see Fig. 1) the second electrode electrically open, as the second electrode is connected to the capacitor and is not associated with the photoelectric conversion performed in the photodiode. Sawada et al. and Nishiyama do not teach the photoelectric conversion circuit as a photodiode formed on a semiconductor substrate of one conductivity type, by joining a semiconductor of another conductivity type and coating a top surface with an insulating film, the first electrode formed by removing a part of the insulating film so that the first electrode is made contact with the semiconductor or another conductivity type. Liang et al. teach (see Fig. 2B) a photodiode with a first region (D,GX) formed on top of a semiconductor substrate (35) of one conductivity type ("P-") by joining a semiconductor (D_b) of another conductivity type ("N+") and

an insulating film (DK) coating the top surface, where the first electrode is formed by removing a part of the insulating film so that the first electrode makes contact with the semiconductor (D_b) of another conductivity type. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the photodiode of Liang et al. in the device of Sawada et al. in view of Nishiyama, provide a sensitive photosensor using standard manufacturing methods.

Regarding Claim 13, Sawada et al. in view of Nishiyama teach the invention as taught in the previous paragraph for Claim 11. Sawada et al. and Nishiyama do not teach the first chip including a first and second region formed on top of a semiconductor substrate with an insulating film coating on top, where the photodiode is formed by removing a part of the insulating film on the first region to form an electrode contacting the first region and a dummy photodiode is formed by removing a part of the insulating film on the second region to form an electrode that covers all of the top portion of the second region. Liang et al. teach (see Fig. 2B) a photodiode with a first region (D,GX) formed on top of a semiconductor substrate (35) of one conductivity type ("P-") by joining a semiconductor (D_b) of another conductivity type ("N+") and an insulating film (DK) coating the top surface of the top chip, where a photodiode is formed by removing a part of the insulating film that coats the first region and forming the first electrode (G_b) so as to make contact with the first region. Liang et al. also teach (see Fig. 11B) a dummy photodiode with a second region (D,GX) formed on top of a semiconductor substrate (35) of one conductivity type ("P-") by joining the semiconductor (D_b) of another conductivity type ("N+"), where a dummy photodiode shielded from light is formed by removing a part of the insulating film that coats the second region and forming a second electrode in such a way that the second electrode is made contact with the second region through the removed part of the insulating film

and a metal plate (MN) covers all of a top portion of the second region. Sawada et al., Nishiyama, and Liang et al. do not teach the photodiode and dummy photodiode on the same substrate or the second electrode combined with the metal plate- however, it is design choice to combine both photodiodes onto a single substrate and combine the metal plate with the electrode in the dummy photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the photoelectric elements of Liang et al. in the device of Sawada et al. in view of Nishiyama, to form a photodiode with a common CMOS manufacturing method and save space by having both photodiodes on the same substrate on the first chip.

11. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al. in view of Nishiyama as applied to claim 11 above, and further in view of Watanabe.

Sawada et al. in view of Nishiyama teach the invention as taught in the previous paragraph for Claim 11. Sawada et al. and Nishiyama do not teach a substrate having a first conductor pattern and a second conductor pattern formed thereon for mounting the fist chip and the second chip thereon, wherein the first wire connects the first electrode to the first input terminal by way of the first conductor pattern and the second wire connects the second electrode to the second input terminal by way of the second electrode pattern. Sawada et al. and Nishiyama also do not teach a first-bonding operation performed on the first and second chips and a second-bonding operation performed on the first and second conductivity patterns, respectively. Watanabe teaches (see Fig. 3) a photoelectric converter module comprising a substrate (43) to mount a photoelectric conversion circuit (11, 30) and an amplified circuit (20) with a first (31a) (see Fig. 4A) and second (31b) conductor pattern, and bonding wires (22) (see

Col. 4, lines 42-47) to connect the conductor patterns to the amplifier (20). Regarding Claim 14, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Sawada et al. in view of Nishiyama with the connection methods taught by Watanabe, to provide an integral photoelectric/amplification device. Regarding Claim 15, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the two wires as two separate bonding operations in the invention of Sawada et al. in view of Nishiyama, as two separate electrical connections are being bonded, providing a lowered risk of chip breakage.

Response to Arguments

In response to Applicant's traversal of the rejection of Claims 1 and 9, the Examiner maintains the rejection of the aforementioned claims. The Applicant argues with respect to Sawada that the differential amplifier is located in an external package as opposed to integrated within a package. The Examiner maintains that the differential amplifier is still within the scope of the device, as the final signal output of the entire device is shown in Fig. 3 as V_{OUT1} and V_{OUT2}, which feeds from the output of the differential amplifier which is directed to a comparator external to Sawada's invention. Hence, the differential amplifier is considered an essential aspect of the invention of Sawada and is therefore a component of the package. In addition, Applicant does not specifically claim noise-cancellation function, but simply provides the limitation of a differential amplifier, which Sawada also teaches. Also, while Fig. 1-3 are schematic diagrams, Fig. 5 and 6 show a physical depiction of the device, and the wires (7,8) which continue through (36,37) are seen as substantially identical in length and substantially parallel, except for the short wire distance between the IC chip (50) and the wires (36,37). Since the wires (36,37) are much longer than the wires (7,8) and the differential amplifier is connected at the bottom end of the wires (36,37) (see Col. 6, lines 12-16), it is deemed that the wires (7, 8, 37, 38) that lead to the amplifier are laid substantially parallel and have substantially identical lengths.

In response to Applicant's traversal of the rejections of Claim 5 and 6, the Examiner maintains the rejections of the aforementioned claims. As stated above, the differential amplifier in the package of Sawada is considered an essential component in the performance of the system and is therefore included within the light-receiving device. In addition, Sawada teaches a dummy photodiode used in place of the equivalent capacitor (see Col. 6, lines 18-20). In regards

to the first and second wires being substantially equal in length and substantially parallel, Sawada teaches the first and second wires being substantially equal in length and substantially parallel, as shown above in the Examiner's response to the traversal of the rejection of Claim 1. Regarding Claim 5, it is not possible for the second electrode to be simultaneously electrically open and also connected physically to the photoelectric conversion circuit.

In response to Applicant's traversal of the rejections of Claim 7 and 8, the Examiner maintains the rejections of the aforementioned claims. Watanabe teaches (see Fig. 3) a substrate (43) to mount the photoelectric conversion circuit (11, 30) and the amplified circuit (20). Watanabe also teaches (see Fig. 4A) a first (31a) and second (31b) conductor pattern, and bonding wires (22) (see Col. 4, lines 42-47) to connect the conductor patterns to the amplifier (20). Since there are two conductor patterns, it is inherent that there are two wires to connect each conductor pattern to each input of the amplifier. In regards to the first and second wires being substantially equal in length and substantially parallel, Sawada teaches the first and second wires being substantially equal in length and substantially parallel, as shown above in the Examiner's response to the traversal of the rejection of Claim 1.

Thus, as set forth above, this final rejection is proper.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (703)308-4881. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

STEPHONE ALLEN
PRIMARY EXAMINER

SY S.Y.
August 23, 2002